Authors: Jim Swonger and Don Koch

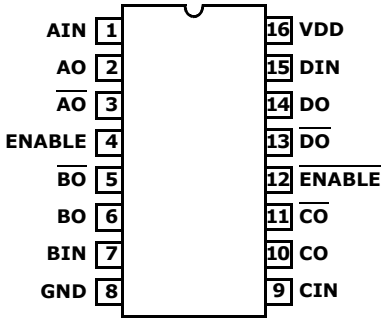
Using the HS-26C(T)31RH Radiation Hardened RS-422 Line Driver

Description

The HS-26C(T)31RH is a radiation hardened RS-422 line driver which incorporates specific performance enhancements while maintaining pin and functional compatibility with commercial 2631 types. The HS-26C31RH has CMOS input levels and the HS-26CT31RH accepts TTL-level signals. The two circuits are identical except for the configuration of the input buffers. The HS-26C31RH has substantially lower output impedance and higher output current capability than commercial types. Short circuit protection to ground is provided by an active output sense circuit. A power-up reset feature inhibits output below 3.5V (typical). These features address requirements particular to the space design community. This Application Note describes the operational characteristics of these features and the differences from commercial 2631 part types.

Pinout

HS-26C(T)31RH
TOP VIEW



Output Characteristics

The output drivers of the HS-26C31RH have been designed to provide a low, constant output impedance over the operating output range. The Z_{OUT} is typically 5Ω. The low impedance allows closer, more repeatable matching to transmission lines.

An output impedance of 5Ω requires a very high output current capability. The BiCMOS output stage consists of a large NMOS sink driver and a PMOS/NPN emitter follower source driver. Both have 4Ω output resistors in series to linearize the output impedance (the bulk of Z_{OUT} comes from the resistor; the driver devices are sized so that their contribution is small). Both the source and sink drivers are capable of current in excess of 500mA, consistent with their Z_{OUT}.

While the drivers have high current capability electrically, the ability of the device to dissipate heat precludes using them in continuous-duty high-current applications. The output current/impedance characteristics are designed to meet transmission-line matching and drive requirements.

The source (high) driver has an output short circuit protection mechanism which protects against output shorts to ground. This IOS limiter operates in a unique manner. Short circuit is sensed as the failure of the output to move above a threshold (typically 1V) within a set time-out (50ns to 100ns). If the output does not move, the high drive is reduced from its initial high level to a lower drive of 120mA typical (compliant with the RS-422 150mA IOS limit). An output which is shorted will trip to the 120mA IOS state when brought below 1V. When the output short is released, the output driver returns to its normal state when the output voltage (driven by the IOS current) rises above 1V. This mechanism allows the output to supply the high currents necessary to present a low output impedance but prevents the driver from being damaged by short circuit conditions.

The presence of the IOS feedback circuit means that there is active circuitry which takes its input from the output pin. There is therefore, a dynamic IDD component deriving from output pin activity as well as from input-controlled transitions. A three-stated part on an active line will draw slightly higher IDD because of this circuit activity. However, the time-averaged IDD in such an application is only 33µA/MHz/channel.

Output Drive Current vs Output Voltage

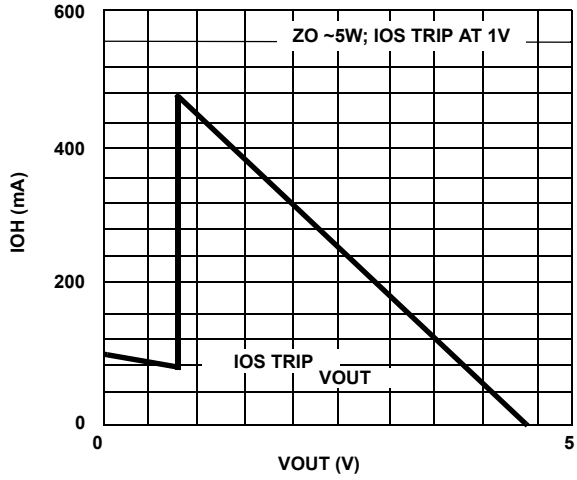


FIGURE 1A. IOH vs VOUT

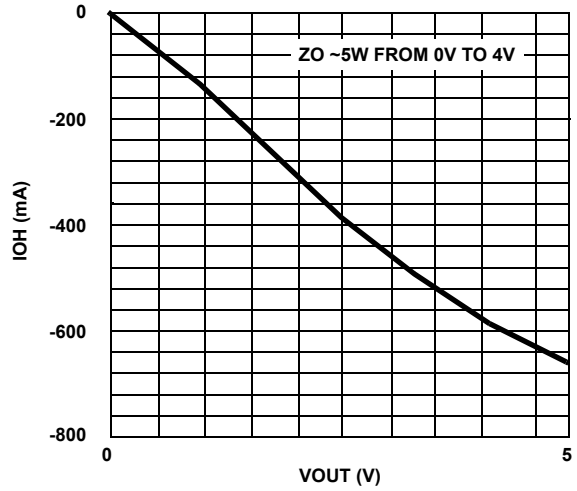


FIGURE 1B. IOL vs VOUT

FIGURE 1.

Power-Up Reset

The HS-26C(T)31RH design includes a power-up "reset" circuit which maintains the outputs in a high-impedance state until the supply voltage rises above a preset threshold, typically 3.5V. This ensures that the outputs will either be under input pin control or will be three-stated.

This feature has value in applications where entire modules or boards are power-strobed to reduce supply demand or for redundancy. Many space applications take this approach. The POR feature provides the capability to power-cycle the circuit without line interference.

The POR enable level was set to keep the outputs three-stated well past the point where the HS-26C(T)31RH becomes functional. The reason for the high threshold is the fact that some customers have reported anomalous behavior in their TTL-based logic circuits (glitches, oscillations, etc.) at lower supply levels where these part types are just becoming active. Since these circuits would be controlling data and enable pins on the HS-26C(T)31RH, it is desirable to block all inputs and maintain output three-state until the control inputs can safely be assumed to be valid and stable. A 3.5V POR level is a good compromise between system stabilization and supply headroom.

The POR circuit has built-in hysteresis to allow more supply headroom once the part is powered up. That is, the POR enables the outputs at 3.5V but does not disable them until the supply falls below 3.2V (typical).

Supply Decoupling

The HS-26C(T)31RH has very high drive current capability. This means, in addition to the desirable ability to quickly drive a large load, a requirement to have that drive current readily available at the supply pins.

The VDD and ground pins of these devices should be bypassed as close to the part as physically possible with capacitors having low ESR and moderate-to-high capacitance. The amount of capacitance scales with the load driven. A minimum of 0.1µF is recommended, and more is suggested.

To derive the theoretical minimum bypass cap required, take all four channels switching in unison. There is an internal transient current demand and a load current demand. Assuming max VDD and 200pF/channel load, with the output swinging from ground to VDD - 1V.

$$I_{INT} = CPD \quad (dv)/(dt)$$
$$I_{INT} = 4(170p) \times \left(\frac{5.5V}{3ns}\right) = 1.2A \qquad \text{(EQ. 1)}$$

$$I_{LOAD} = C_{LOAD} \quad (dv)/(dt)$$
$$I_{LOAD} = 4(200p) \times \left(\frac{(4.5)V}{5ns}\right) = 720mA \qquad \text{(EQ. 2)}$$

$$I_{DD(PK)} = 2A \qquad duration 5ns \qquad \text{(EQ. 3)}$$

Applying a 2A/5ns rectangular pulse to a 0.1µF capacitor will remove 1E - 8 Coulomb of charge. Using DQ = CdV, Equation 4 gives:

$$1E-8 = 1E-7 dV \text{ or } dV = 0.1V \qquad \text{(EQ. 4)}$$

In real applications, however, there are additional considerations. In particular, the resistance and inductance of board traces have the potential to slow the maximum current edge rate, thereby collapsing the available VDD at the part or raising the ground level. Inductance also has the potential to form a resonant supply/ground circuit which can degrade noise margins and timing if ringing is severe enough to approach the noise margin levels. As with other high speed/high drive logic types, proper board design is a factor in obtaining optimum performance.

Transmission Lines

The RS-422 transmission line is a twisted-pair, 100Ω line standard. The standard RS-422 load is a 100Ω shunt termination and three 100pF capacitors, one between pins and one from each output pin to ground. This is intended to model the load presented by a cable attached to the pins.

In satellite applications the use of shunt termination is unappealing due to the high amount of current required to hold a line signal voltage against the shunt resistance: 20mA or more per channel, typically 40mA, even when the signal is doing nothing at all. For this reason, these applications typically use source (or series) termination resistors to match the transmission line impedance.

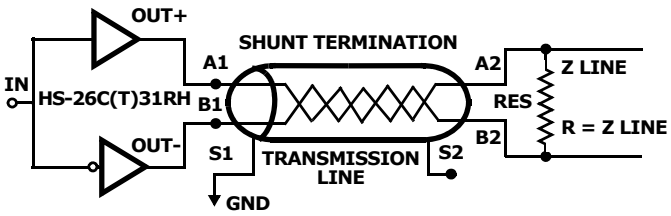


FIGURE 2.

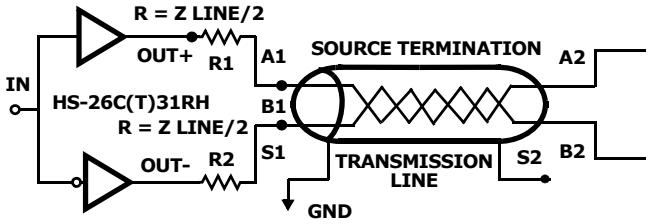


FIGURE 3.

Source termination depends more heavily on the quality of line driver characteristics and impedance matching than shunt termination. This is due in large part to the absence of any DC return path for the signals. The drivers excite the line pair in antiphase. If this antiphase is perfect, the lines cancel perfectly and there is no current in the shielding and no radiated noise from the line. If the matching of the line impedance is perfect, the transition will be completed on the first reflection.

If the signal transitions of the true and complement drivers are separated in time, there will be a different current generated by the failure of the lines fields to cancel each other; this difference current will run in the shield, which becomes a third line rather than a passive covering. This unshielded current is undesirable; it produces EMI which can degrade the performance of nearby circuitry. The timing skew specification of the RS-422 Specification is intended to limit the amount of time difference. A typical HS-26C(T)31RH has less than 1ns of skew.

If the line impedance is not properly matched, the waveform at the far end of the line will not settle to its final value immediately. This compromises noise margin and can cause odd behavior if the next transition is applied before the first has settled. A shunt resistor of the same resistance as the characteristic line impedance or two series resistors, each Z/2, are ideal. A terminating resistor larger than ZLINE will produce a far-end waveform which is "overdamped"; it steps most of the way to the final value, a bit more on the next reflection, never quite getting there but getting closer. A low value for the matching resistor will act "underdamped"; the far end will overshoot, then undershoot, hunting around the final value. This behavior is more dangerous because in severe cases the undershoot may actually recross the far end receiver's input threshold and produce multiple logic transitions before it settles out. In practice, the percentage of mismatch corresponds pretty well to the amount of overshoot or undershoot.

This requirement for good line matching is the primary reason for the high output drive capability/low output impedance design of the HS-26C(T)31RH. By minimizing the amount and variability of the impedance inside the device, the total drive impedance (the sum of internal impedance and external matching) is less subject to variability from supply, temperature and radiation. This allows tighter matching and better transmission line performance.

Power Dissipation

The HS-26C(T)31RH dissipates about 100µA IDD current at standby (limit = 500µA). Most of this is in the analog power-up reset circuitry.

Operating current at frequency is the sum of the standby current and the dynamic operating current given by (CPD)(VDD) (frequency). For the HS-26C(T)31RH the CPD (per active channel) is 170pF.

Cross-Strapping

In space systems it is vital to have a data communications bus structure which provides resistance to single point failures. One common technique is the use of redundant bus drivers and receivers in parallel, sometimes called cross-strapping. In this arrangement one driver and receiver are active and another pair is quiescent. The desire to minimize power leads to the need to power down the redundant circuits. This poses a problem for typical CMOS output structures and input protection circuits. The parasitic diodes in the P-Channel output drivers and the input clamp diodes will tend to clamp the signal unless the supply voltage to the quiescent parts remains above the bus signal range.

The HS-26C(T)31RH transmitter provides RS-422-compliant output characteristic, including power-off isolation. The output stage presents a high impedance to the line with power off (VDD < 3V). This prevents any significant amount of current flow over an output voltage range of 0.25V to 6V with respect to device ground.

The use of a BiCMOS output stage provides an output characteristic very similar to LSTTL devices and superior to standard CMOS. Figure 4 shows what the NPN, NMOS and PMOS device physical structures look like. Figure 4

illustrates the four standard output topologies and their associated parasitic diodes.

The standard P-Well CMOS structure presents an undesirable characteristic to the line when the supply is at 0V. This is due to the P-Channel drivers parasitic drain-body diode, which becomes forward-biased at voltages above ground (see Figure 5A).

N-Channel source-follower high side drivers and NPN-based output drivers have parasitic diodes which remain reverse-biased with VDD at 0V and output voltages above ground. These output types will not conduct until the E-B or S-B diodes break down, typically above 7V (see Figures 5B and 5C).

The HS-26C31RH line driver is produced in a radiation hardened CMOS process but uses a NPN bipolar output driver to provide both high output drive and power-off output isolation. The output can be run from ground to over 6V without significant leakage, with the supply off, unlike standard CMOS logic types. This allows the outputs of active and inactive drivers to be paralleled without complications (see Figure 5D).

The HS-26C32RH line receiver has an input structure which provides a ±10V maximum input signal range with respect to device ground. The input impedance of the receiver is typically 10,000Ω, with no clamping devices at the pin. A powered-down device simply adds its input impedance in parallel to the other devices on the line.

Lab tests verify the difference in behavior between a standard CMOS input and output with power off and the HS-26C31RH and HS-26C32RH devices line inputs and outputs. The inactive CMOS devices clamp whatever line they are attached to at less than a volt, drawing many mA. The line pins of the Intersil RS-422 chip set are well-behaved, acting as a three-state output and a 10kΩ input.

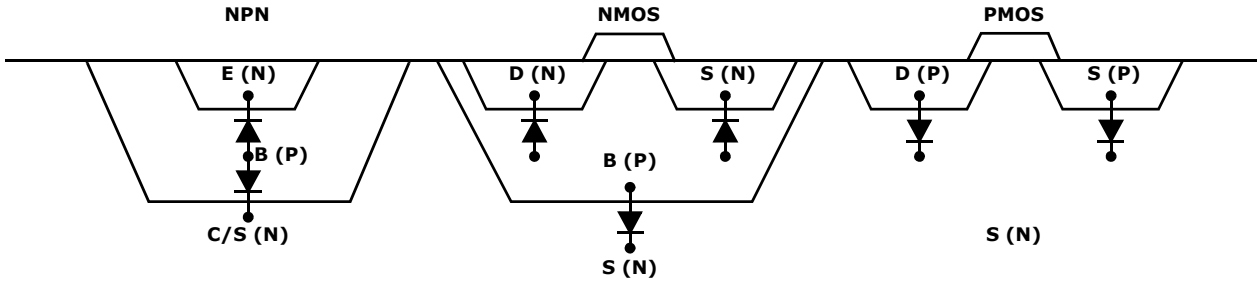


FIGURE 4. NPN, NMOS AND PMOS DEVICE PHYSICAL STRUCTURES

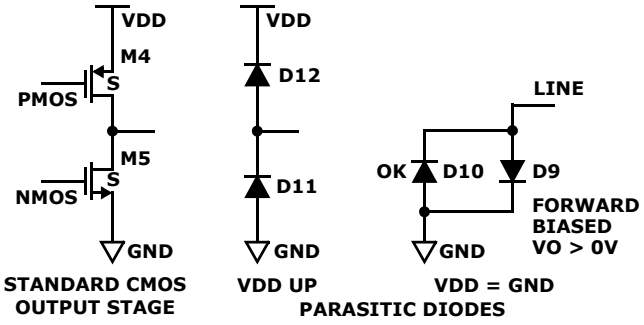


FIGURE 5A. STANDARD CMOS OUTPUT STAGE

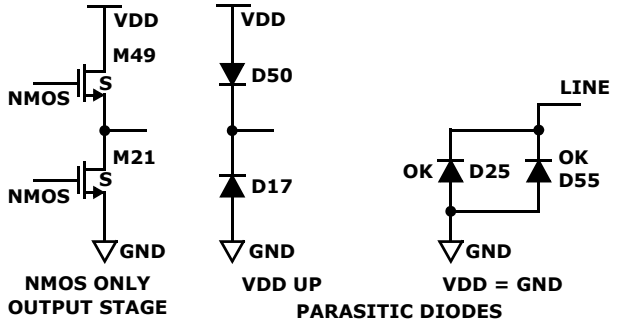


FIGURE 5B. NMOS ONLY OUTPUT STAGE

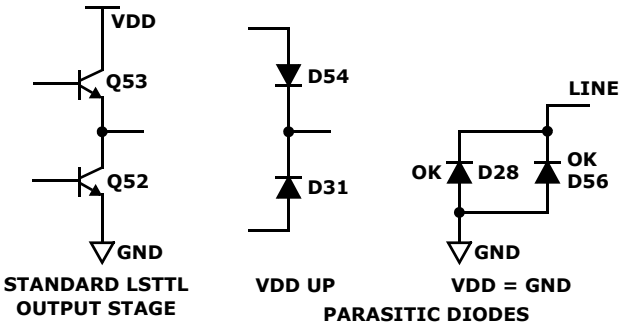


FIGURE 5C. STANDARD LSTTL OUTPUT STAGE

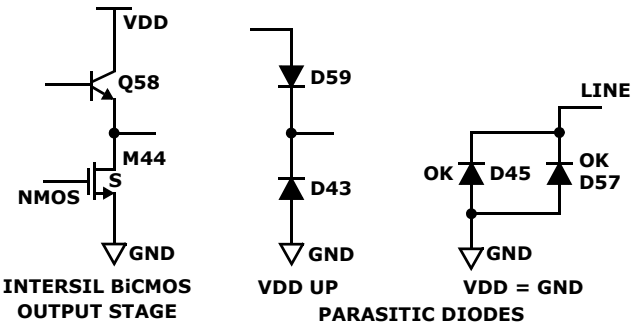


FIGURE 5D. INTERSIL BICMOS OUTPUT STAGE

FIGURE 5. FOUR STANDARD OUTPUT TOPOLOGIES

System Noise

Another primary benefit of a balanced, differential line standard such as RS-422 is the cancellation of radiated EMI from the data lines. A shielded twisted-pair data line has primary EMI cancellation by virtue of the antiphase signals and Faraday shielding as well. In applications, where sensitive analog circuitry has to reside near the data bus, this type of bus standard can significantly improve system noise levels and signal quality.

Using this chip set, a 10MHz, low power, quiet bus system with cross-strapped redundant data paths can be implemented easily. The Intersil radiation-hardened CMOS solution cuts power compared to bipolar chip sets and allows configurations not possible with standard CMOS logic.

The large voltage swings, low typical line impedance and differential bus also provide superior immunity to both supply and radiatively-coupled noise. The normal signal span is 8V (+4 to -4) for the HS-26C31/32RH, less than 5V for standard single-ended CMOS and less than 4V for LSTTL. In addition, the HS-26C32RH can tolerate differences between driver and receiver ground levels which would render standard logic either unreliable or completely nonfunctional. For example, an LSTTL or CMOS input whose ground supply is more than 1V below the driving device's may never switch because its VIL(min) level cannot be met. The HS-26C32RH functions properly with its inputs ±7V from device ground. This also minimizes the chances of ground bounce or supply spikes causing false logic states.

Substrate Connection

The substrate of the HS-26C(T)31RH circuits is connected internally to the VDD pin. If the HS-26C(T)31RH is used in die form for hybrid applications, the die should be mounted to an electrically isolated surface. If there is any electrical connection to the back side of the die, there will be a low value resistance to the VDD pin. However, the value of the resistance of the substrate and mounting material are not necessarily low or well enough controlled to use as a supply feed.

Summary of 2631 Type Lab Comparison Results

OUTPUT IMPEDANCE

The Intersil HS-26CT31RH has a constant output impedance of 5Ω over its output range.

The commercial LS and CMOS part types have output impedances which are not constant; they change from 5Ω to 10Ω to >100Ω over the output swing.

OUTPUT CURRENT MAXIMUM

The HS-26CT31RH will source and sink over 500mA (+25°C, 5V). This reduces loading effects on timing. It also increases signal strength at higher data rates.

The commercial LS and CMOS parts are limited to approximately 100mA.

OUTPUT SHORT CIRCUIT CURRENT

The HS-26CT31RH provides an output short circuit current limit of 130mA into a true short-to-ground. In other conditions full output current is permitted.

Commercial LS and CMOS parts IOS and maximum drive current are the same.

TRANSMISSION LINE PERFORMANCE

HS-26CT31RH provides stronger signal at far end of line, less amplitude degradation with increasing frequency.

Radiated noise (shield current) is equivalent to other types.

RADIATION

The HS-26C(T)31RH and HS-26C(T)32RH have been fully characterized to 300k RAD total dose. A sample of each wafer lot is evaluated to 300k RAD (Si) total dose, and all post rad electricals (in accordance with the datasheet) must pass.

In addition, Single Event Upset (SEU) and Single Event Latch-up (SEL) testing on these two parts demonstrate that the SEU and SEL thresholds are each >80 MEV/mg/cm^2. The testing was performed by NASA Goddard SFC, and is published in the 1994 IEEE Radiation Effects Data Workshop. (IEEE Publication # 94TH06841, "Single Event Effect Proton and Heavy Ion Test Results for Candidate Spacecraft Electronics", by K. LaBel et al).

CONCLUSION

The Intersil HS-26CT31RH provides superior hardness to the commercial bipolar and CMOS types tested. Power dissipation is less than CMOS or bipolar types up to 1MHz unloaded. Higher output signal strength consumes slightly more power in load. Intersil RH CMOS part can run three channels fully loaded at 10MHz on less current than an unloaded LS part at DC.

TABLE 1. PRE-RAD UNLOADED ICC AND CPD

PART TYPE	ICC DC (mA)	ICC 1MHz (mA) (Note 1)	ICC 10MHz (mA) (Note 1)	CPD (pF/CHANNEL) (Note 2)
HS-26CT31RH	0.3	1.0	8.7	170
DS26C31CN	1.5	2.5	4.7	65
AM26LS31CN	67.5	68.7	82.4	300

NOTES:

1. One channel active at specified frequency.
2. CPD = (ICC 10M-ICCDC)/(5.0V x 10MHz).

TABLE 2. ICC, 20 FEET OF 77Ω LINE (Note 3)

PART TYPE	ICC 1MHz (mA)	ICC 10MHz (mA)
HS-26CT31RH	11.5	18.2
DS26C31CN	11.3	14.5
AM26LS31CN	73.5	89.5

NOTE:

3. One channel active at specified frequency.

TABLE 3. 1MHz ICC, 20 FEET OF 77Ω LINE (Note 4)

PART TYPE	300k RAD (mA)
HS-26CT31RH	12.0
DS26C31CN	12.2
AM26LS31CN	75.3

NOTE:

4. One channel active at specified frequency.